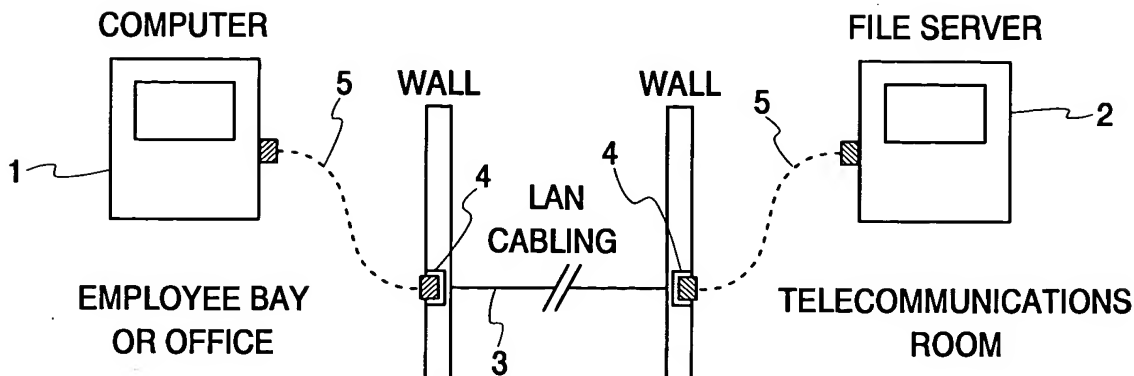
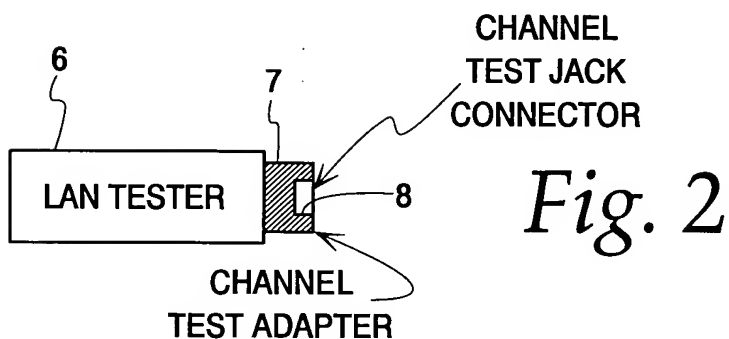


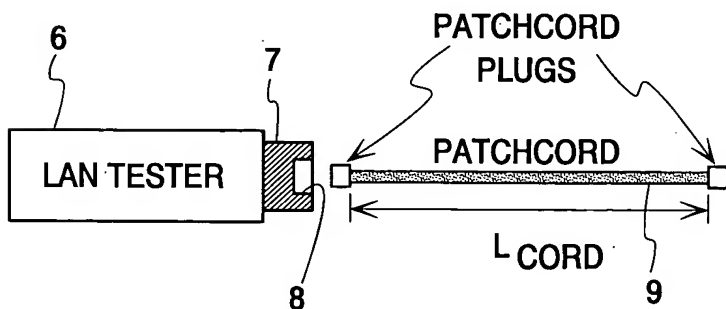
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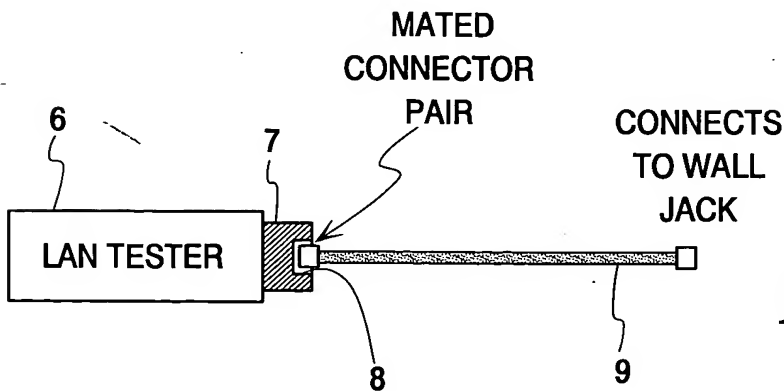
*Fig. 1*



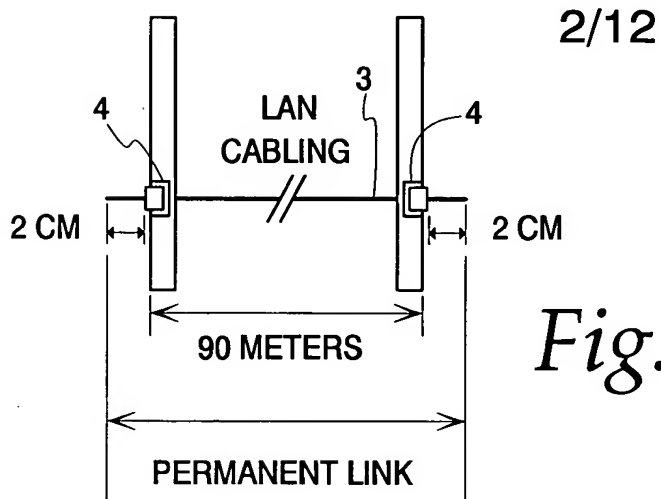
*Fig. 2*



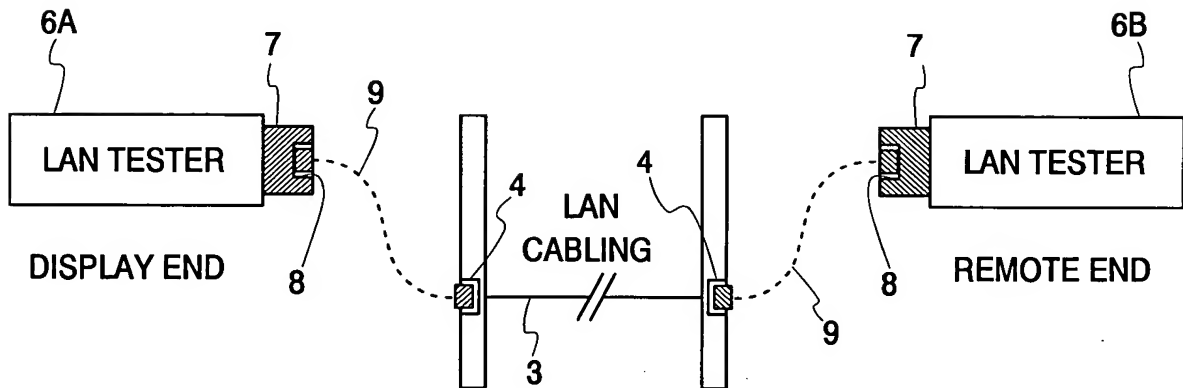
*Fig. 3*



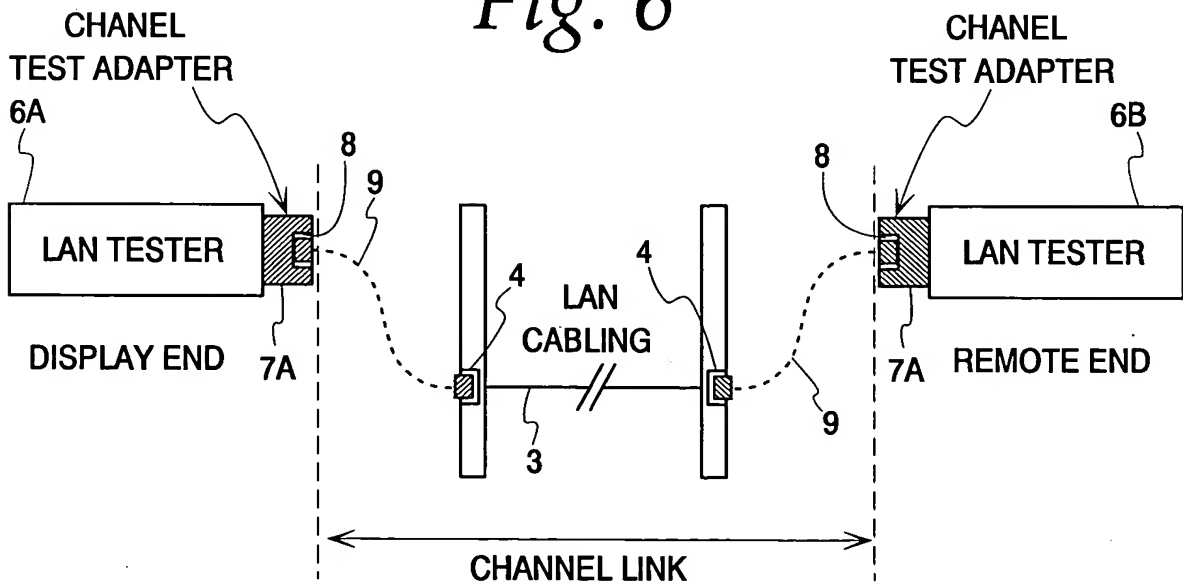
*Fig. 4*



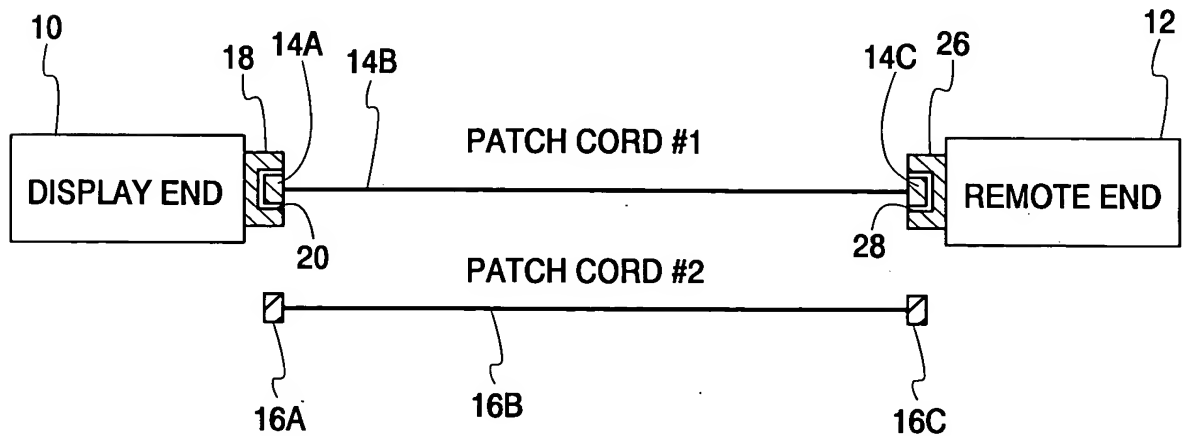
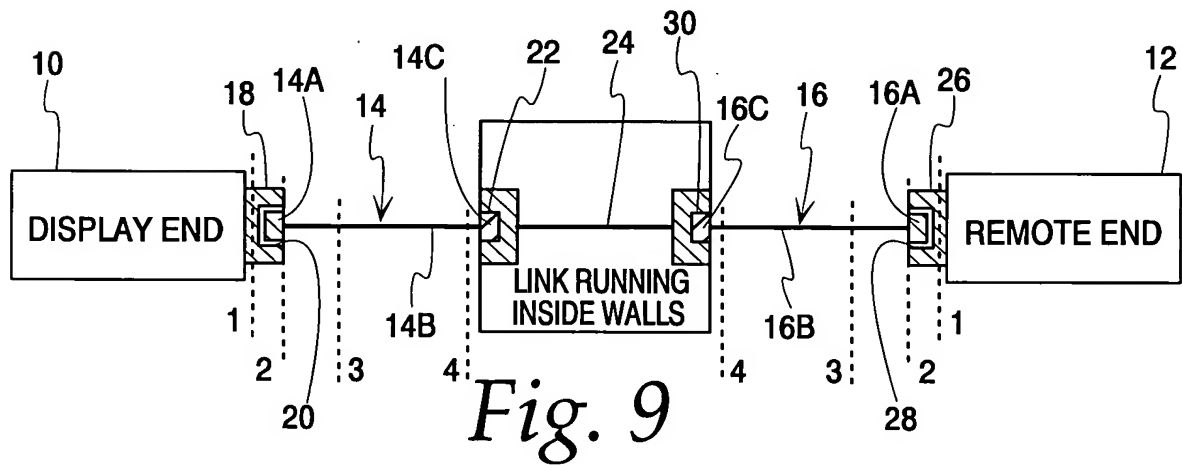
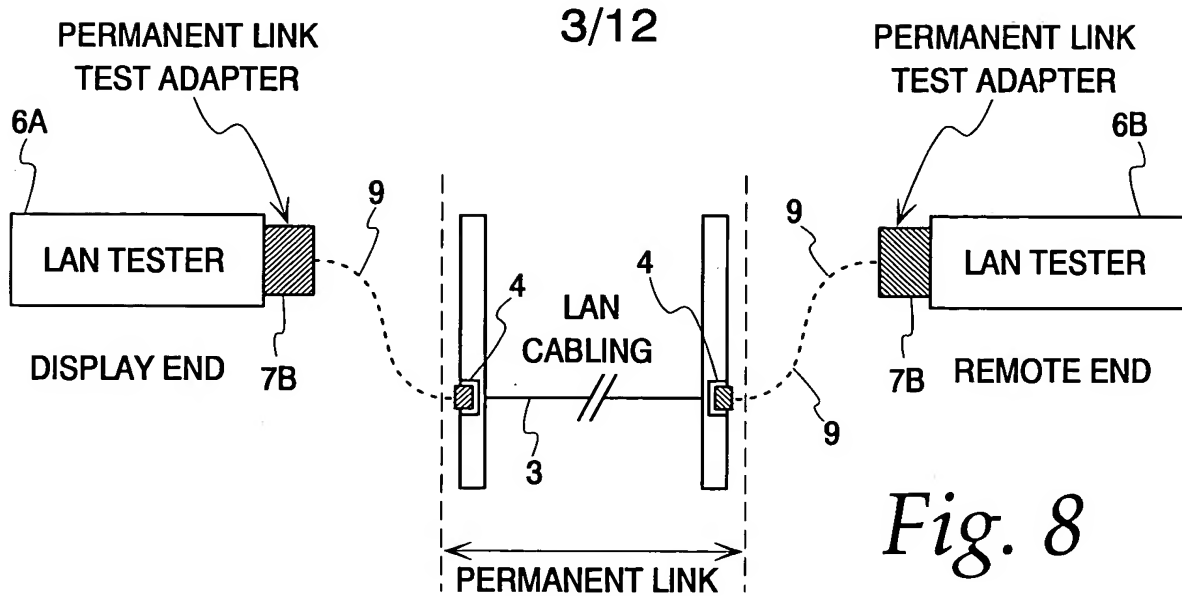
*Fig. 5*



*Fig. 6*



*Fig. 7*



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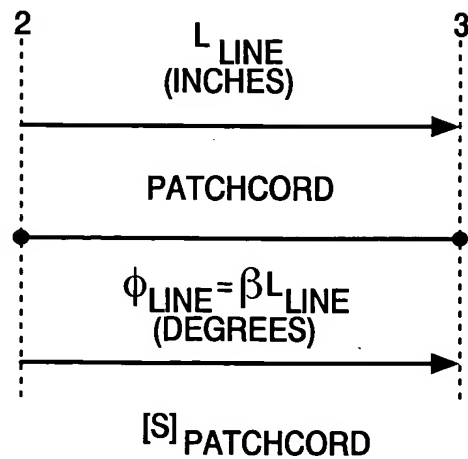
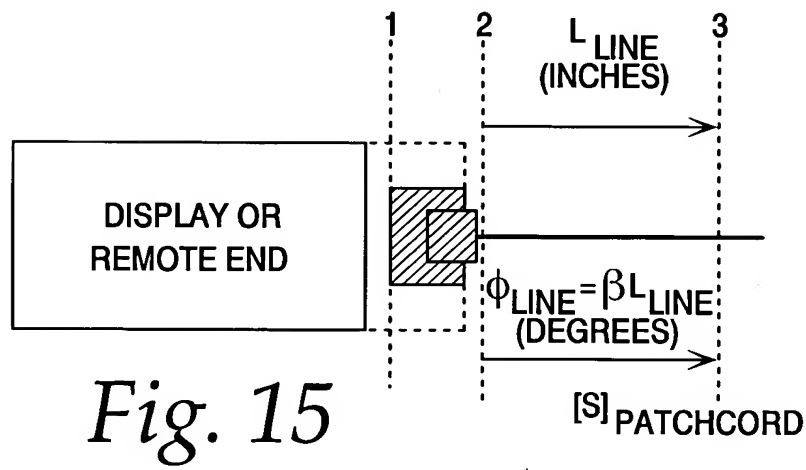
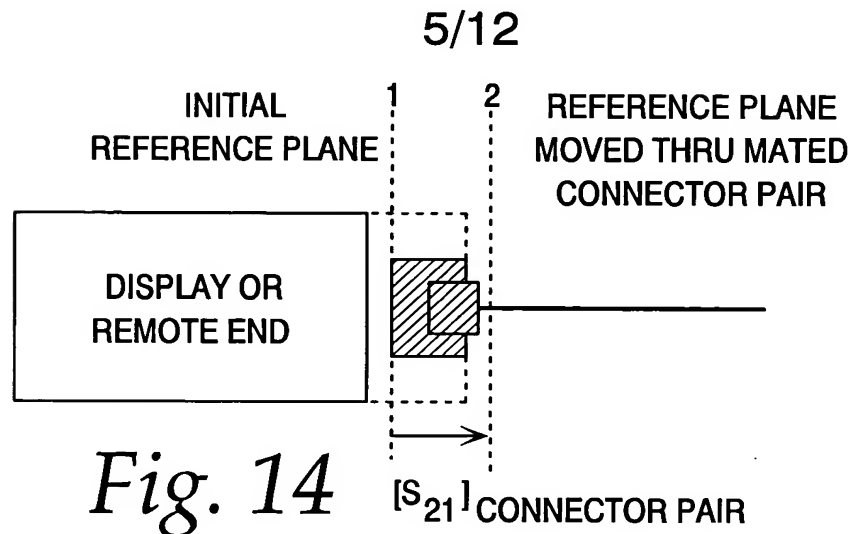
Figure 11 is a graph showing the ratio of drive voltage to measured voltage,  $\frac{V_{Drive_i}}{V_{Meas_i}}$ , versus frequency  $f_i$ . The solid line represents the theoretical response, and the dashed line represents the measured response. The measured response shows a resonance peak at  $f_i = 0.000$  and a resonance dip at  $f_i = 450.000$ .

Fig. 11

*Fig. 12*

Fig. 13

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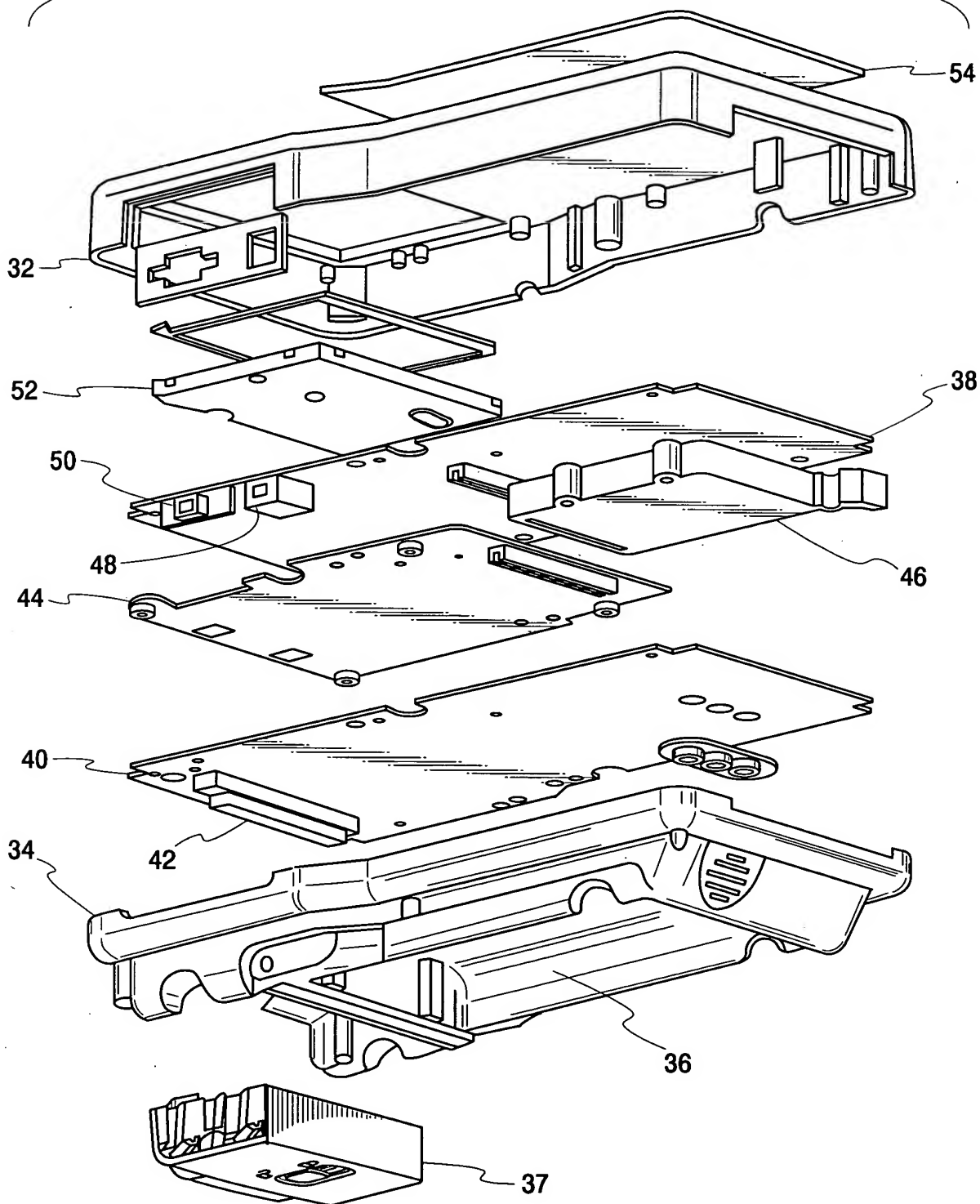


*Fig. 16*

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*Fig. 17*



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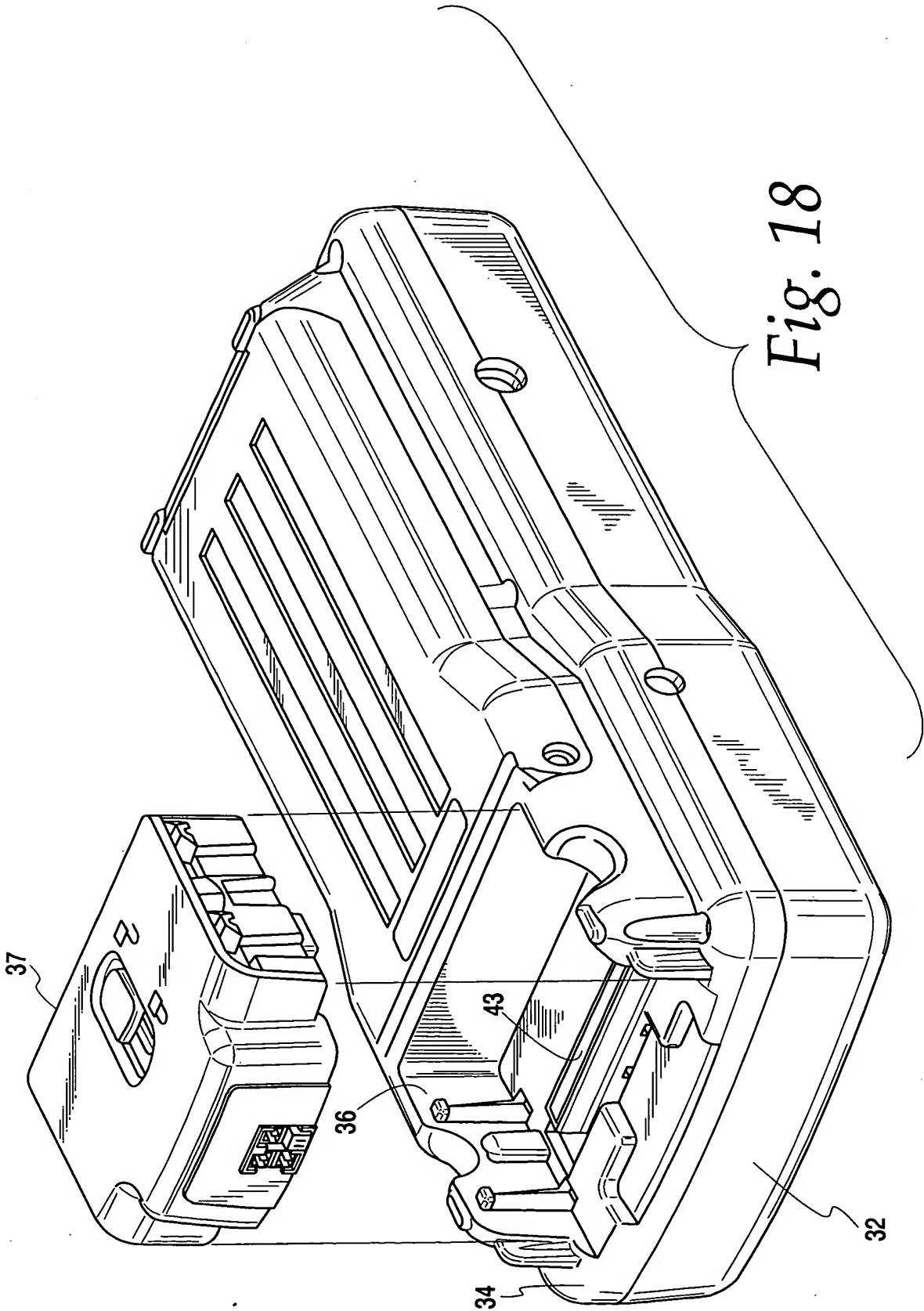


Fig. 18

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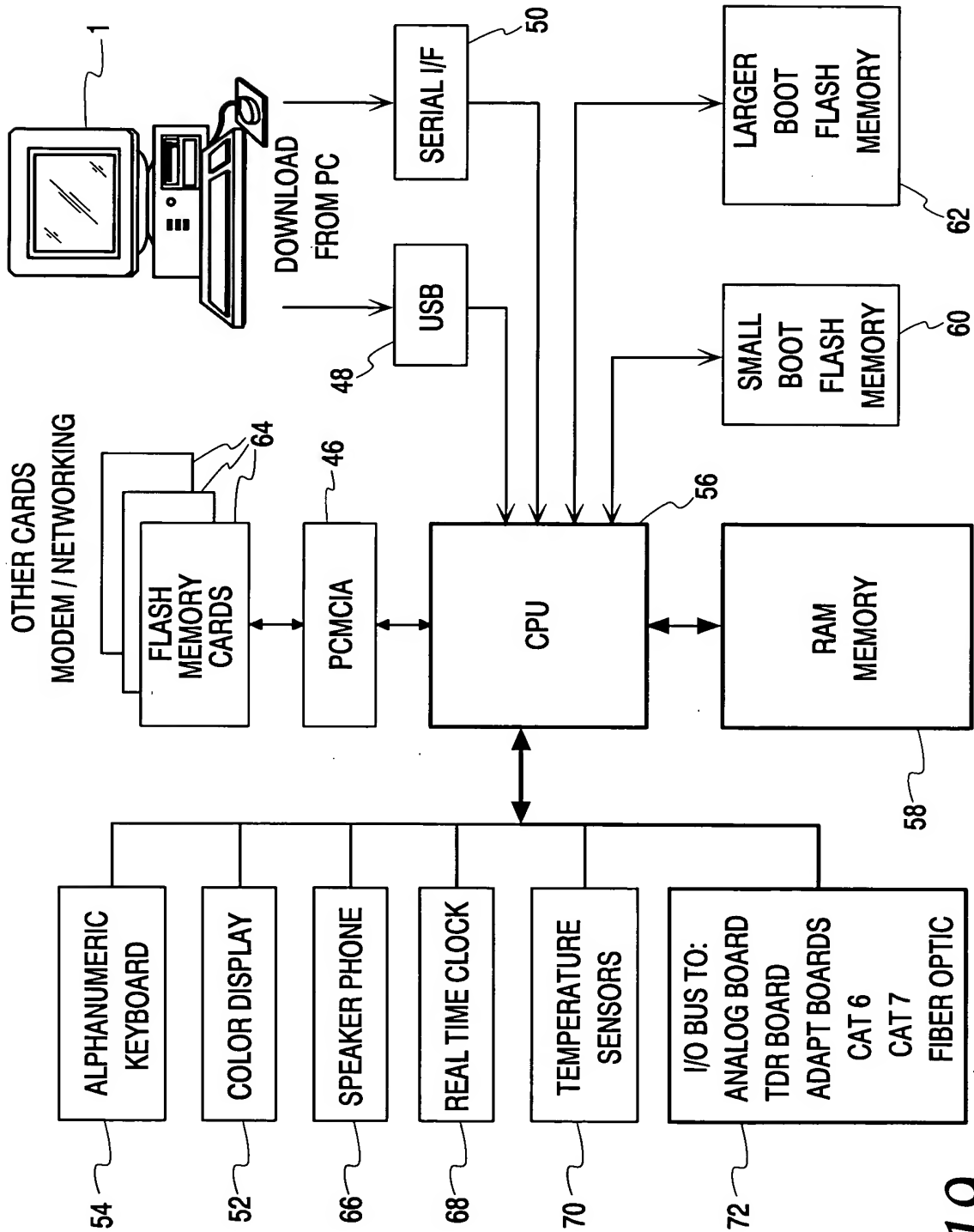
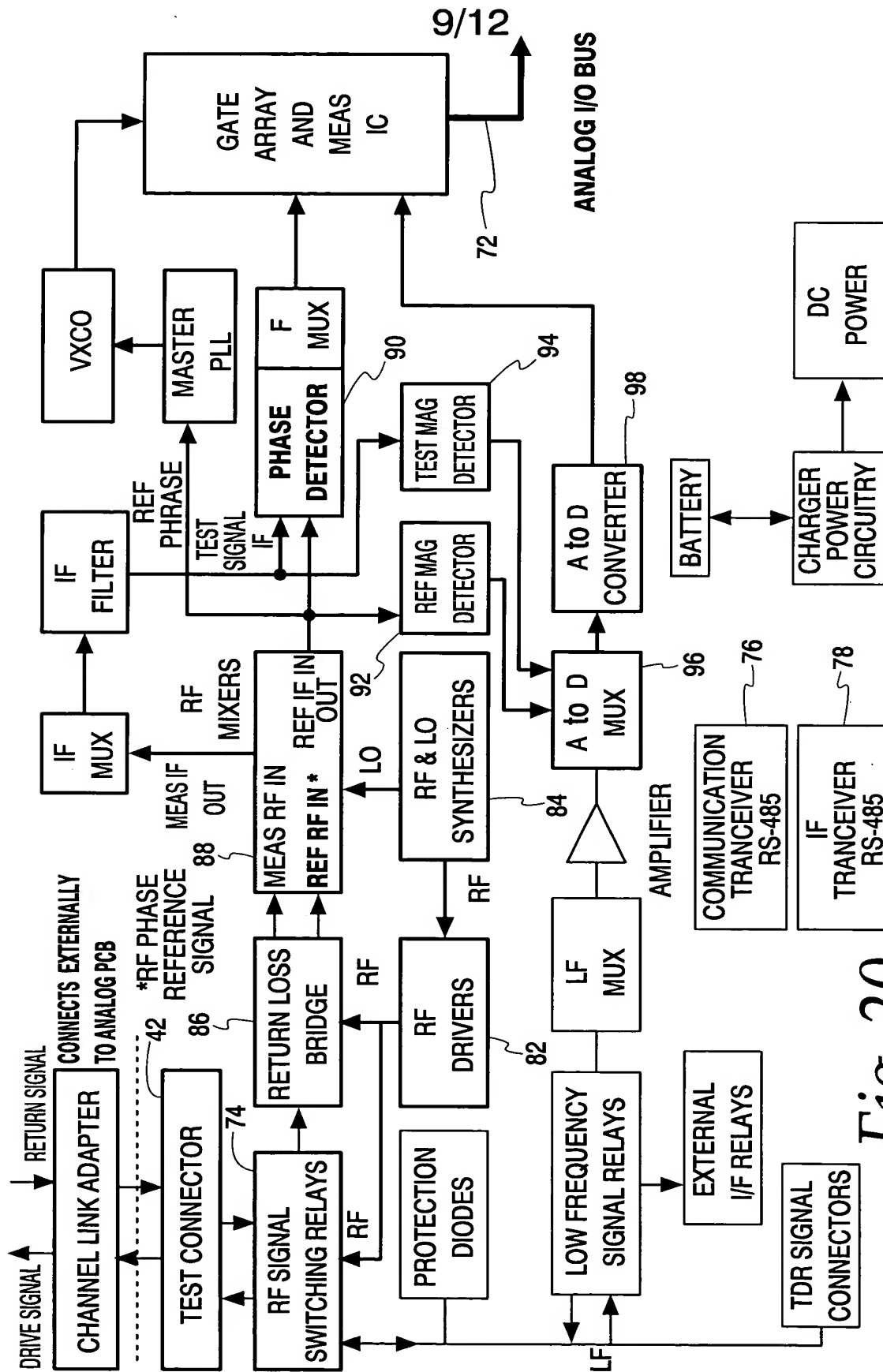


Fig. 19  
 LAN Tester Digital Control Circuit Block Diagram

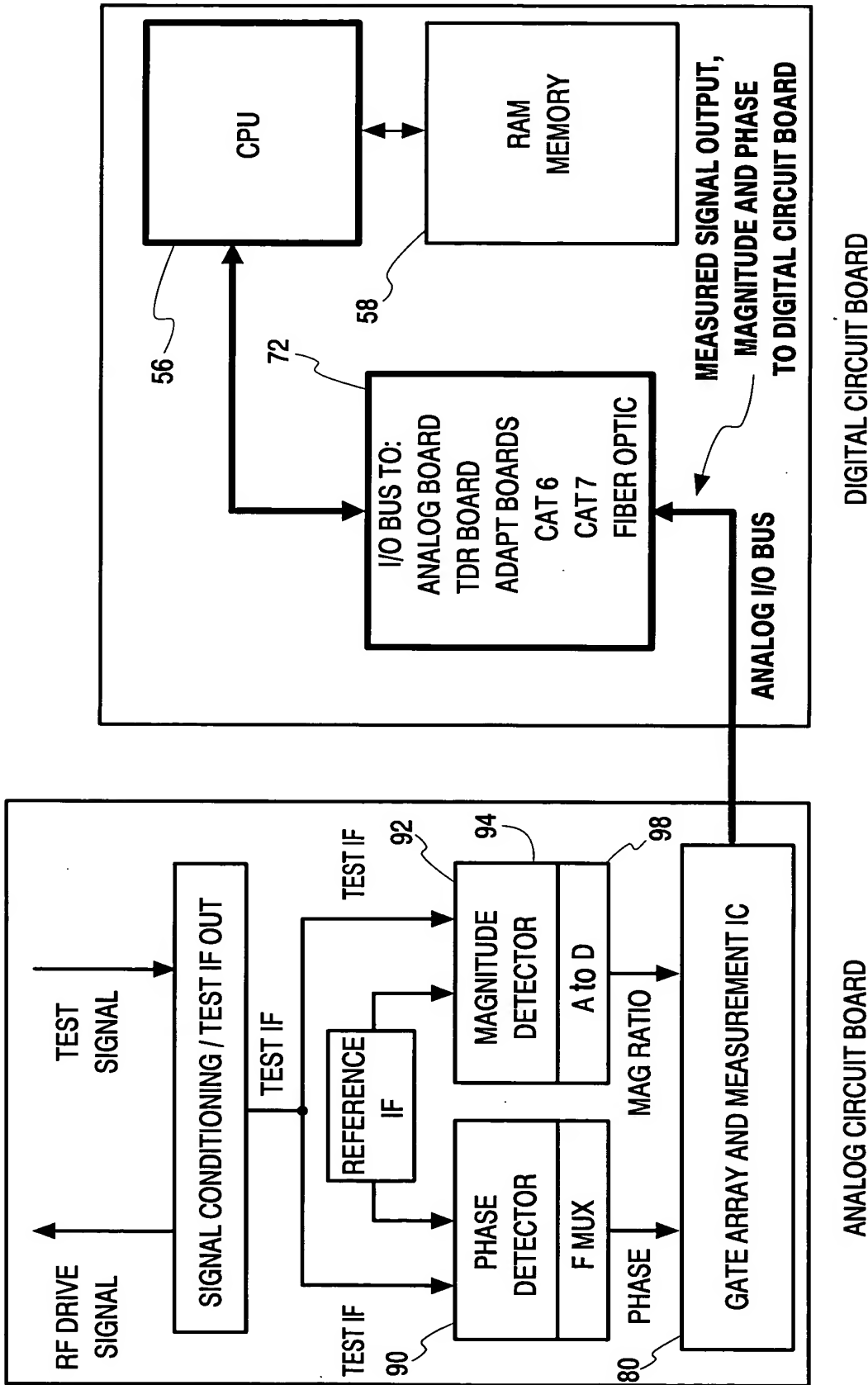


**Fig. 20**

LAN Tester Analog Circuit Block Diagram

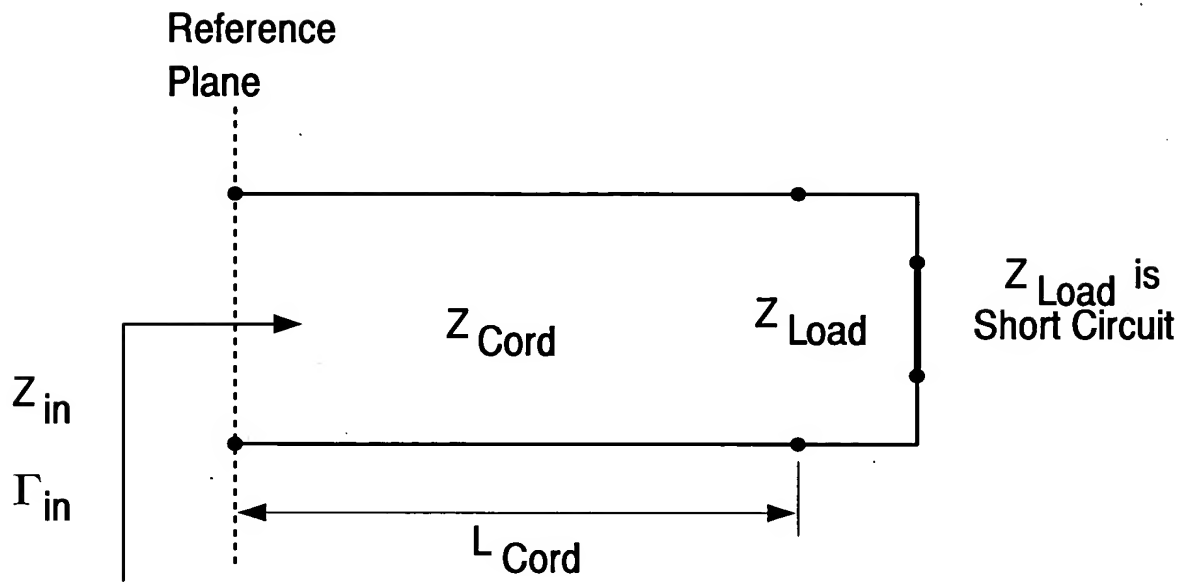
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graph LR; A[FRANCEVEH RS-485] --> B[POWER CIRCUITRY]; B --> C[POWER]
```

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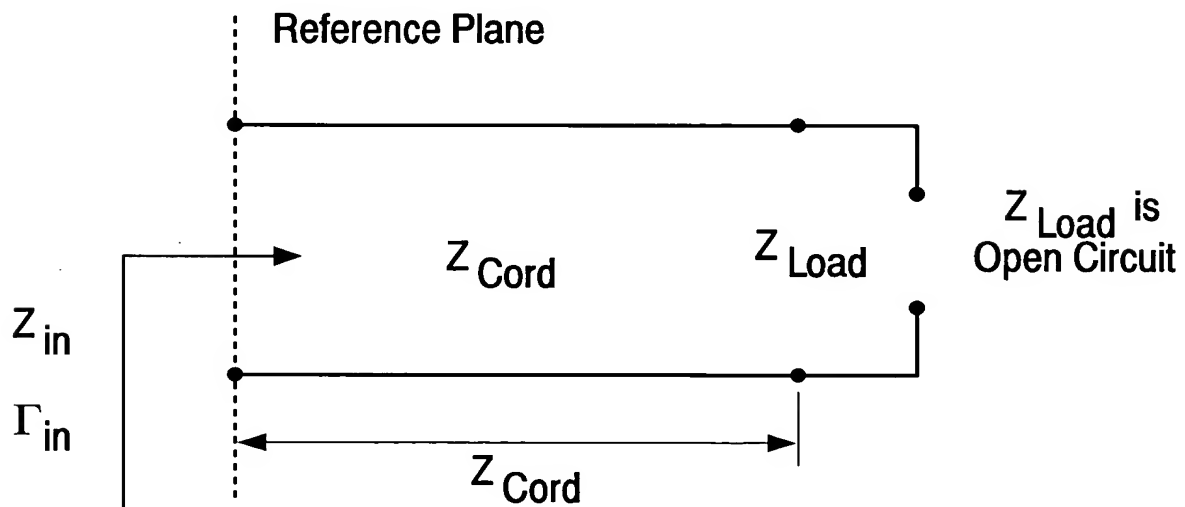


*Fig. 21* LAN Tester Detailed Phase Measurement Block Diagram

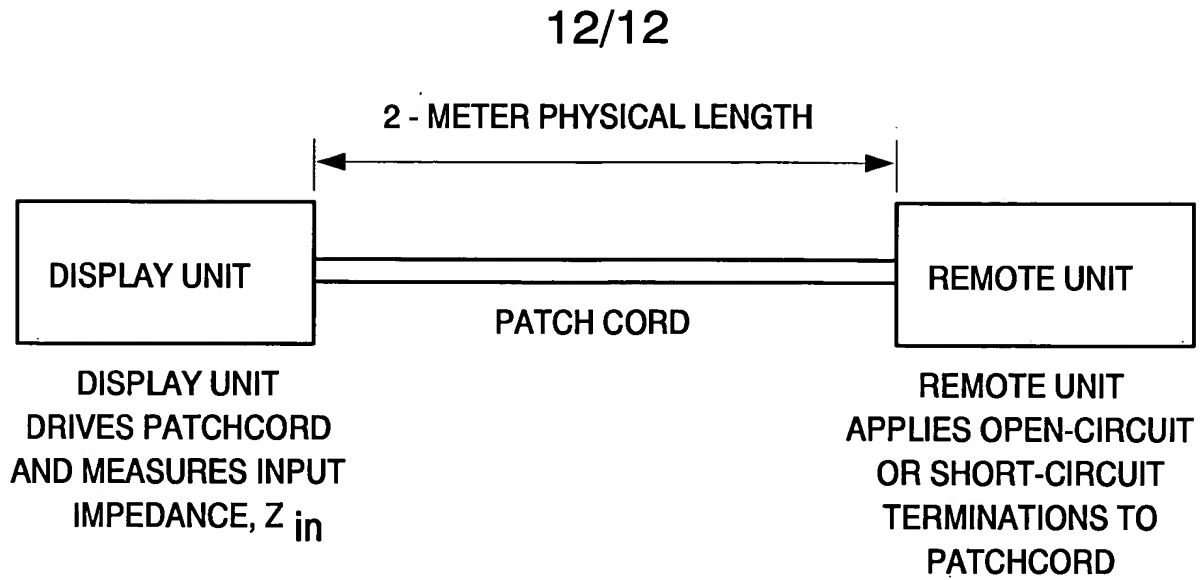
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*Fig. 22* Patch Cord with Short-Circuit Load



*Fig. 23* Patch Cord with Open-Circuit Load



*Fig. 24* PATCHCORD PHYSICAL LENGTH MEASUREMENT TEST CONFIGURATION

